

## ABSTRACT OF THE DISCLOSURE

A semiconductor memory is provided with a defect recovery scheme featuring a redundancy circuit. The memory array in the memory has a plurality of word lines, a plurality of bit lines, a spare bit line, and a plurality of memory cells. The redundancy circuit includes one or more comparing circuits having programmable elements which function as a memory for storing therein a defective address existing in the memory array. The programmable elements of the redundancy circuit can be programmed in accordance with any of a number of different types of defect modes. Each comparing circuit of the redundancy circuit compares information (data) inputted therein, for example, the column and row addresses which may be under the control of an address multiplex system, with that programmed in the programmable elements of the comparing circuit. On the basis of this comparison, an appropriate defect recovery is effected.